

REMARKS

I. Status of the Application

Claims 15, 16, 19-22, 25, 26, 28 and 34-38 are pending in this application. In the February 12, 2007 Office Action, the Examiner:

A. Rejected claims 15, 19-22, 25, 26, 34 and 36-38 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,573,776 to Miyamoto (hereinafter “Miyamoto”) in view of U.S. Patent No. 6,229,364 to Dortu et al. (hereinafter “Dortu”).

B. Rejected claims 16, 28 and 35 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Miyamoto in view of Dortu in further view of U.S. Patent No. 6,208,183 to Li et al. (hereinafter, “Li”).

In this response, applicants have amended claims 15 and 22. Applicants respectfully submit that the amendments place the claims in a condition for allowance. Applicants earnestly solicit reconsideration of pending claims 15, 16, 19-22, 25, 26, 28 and 34-38 in view of the foregoing amendments and the following remarks.

II. Independent Claims 15 and 22 are Patentable Over the Prior Art

In the April 6, 2006 Final Office Action, the Examiner rejected independent claims 15 and 22 as allegedly being unpatentable over Miyamoto in view of Dortu. For reasons discussed below in detail, it is respectfully submitted that obviousness rejection of claims 15 and 22, as amended, should be withdrawn.

A. Claim 15

Claims 15 is directed to a delay lock loop apparatus which can be adapted for use with a broad range of externally generated clock signals. Claim 15 has been amended to clarify that the different second delay elements providing different delay times for the second delay element for different frequency ranges. (See Specification as filed, page 10, lines 7-8). Thus, the apparatus includes a delay device, a feedback device, a frequency detection device and a phase difference detection device. The delay device comprises first and second delay elements. The second delay element comprises different second delay elements providing different delay times for the second delay element for different frequency ranges. At least one second delay element is for low frequency ranges of the clock signal, and at least one further second delay element is for high frequency ranges of the clock signal.

1. Neither Miyamoto Nor Dortu Disclose At Least One Further Second Delay Element for High Frequencies

Neither Miyamoto nor Dortu disclose at least one further second delay element for high frequencies. Conversely, Miyamoto and Dortu each disclose the use of the same delay elements for both low and high frequencies. In the office action, the Examiner stated, and Applicant agrees, that “Miyamoto discloses the same delay elements whose time delay is controlled to accommodate both low and high frequency input signals.” Dortu was cited as disclosing a delay having different delay elements for low and high frequencies such that different sets of inverter pairs may be selected for different frequencies. (Office Action, page 6). Applicant submits that this is a mischaracterization of Dortu. There is no disclosure in

Dortu of “at least one second delay element is for low frequency ranges of the clock signal, and at least one further second delay element is for high frequency ranges.”

Dortu discloses a delay circuit that includes a delay line of inverters (Dortu, col. 5, lines 55-60). The delay units 408 of Dortu each include a pair of inverters for providing an appropriate delay to the input periodic signal. (Dortu, col. 5, lines 63-65). Thus, the input clock signal IN is sequentially transferred through each of the delay units 408. As is known to those skilled in the art, the inverters of the delay line, and thus, each delay unit 408, are configured to incrementally increase the delay time of the input signal as the signal passes through the delay line.

In Dortu, the same delay units 408 are for use with all frequency ranges. Each of the inverters of the delay lines of Dortu are connected to a supply voltage VDD. In order to accommodate different frequencies, the supply voltage VDD is adjusted to modify the incremental delay of the inverters. (Dortu, col. 5, lines 20-23). The VDD may be set to a particular value to adjust delay line 400 for use with predetermined frequencies. (Dortu, col. 6, lines 5-10). For example, a first voltage for VDD is used for a first frequency and a second voltage for VDD is used for a second frequency. (Dortu, col. 6, lines 9-11). Therefore, Dortu discloses a delay circuit that is similar to Miyamoto in which the same delay elements are controlled to accommodate both low and high frequency input signals.

Moreover, in a delay locked loop (DLL), high frequency clock signals require low delay times and low frequency clock signals require high delay times. Because a delay line is configured to increase the delay as the clock signal is sequentially transferred through the inverters of the delay line, the inverters that are operable to provide the delay times for the high frequency clock signals (lowest delay time) are at the start of the delay line. Thus, the

delay elements of the delay lines of Miyamoto and Dortu that are for use with high frequencies are found at the beginnings of the respective delay lines. In order to satisfy the limitation of at least one further second delay element for high frequency ranges, a second delay line of inverters would have to be provided. Neither Miyamoto nor Dortu disclose the use of different delay lines for different frequencies.

2. Neither Miyamoto nor Dortu Disclose Delay Elements for Providing Different Delay Times for Different Frequencies

Neither Miyamoto nor Dortu disclose “delay elements providing different delay times for the second delay element for different frequency ranges.” As described above, each reference, Miyamoto and Dortu, disclose a delay circuit that includes delay elements for incrementally increasing a delay of an input signal. Thus, each delay element of the delay circuits of Miyamoto and Dortu adds a unit of delay to the signal. In order to control the total delay of the delay circuit, each delay element is likely configured to add the same delay to the signal.

In Miyamoto and Dortu, the delay is adjusted by selecting the number of delay elements to include in the delay. (Miyamoto, col. 16, lines 24-27, Dortu, col. 5, lines 65-67). Therefore, in Miyamoto and Dortu, the different delay times are provided for different frequency ranges by selecting the number of delay elements to include in the delay. For example, as described in Miyamoto, as the frequency of the input signal decreases, the frequency detection circuit selects a later one of the signals on the output nodes of the variable delay 402. (Miyamoto, col. 16, lines 25-27). There is no disclosure in Miyamoto or Dortu

that the individual delay elements have different delay times corresponding to different frequency ranges.

3. Conclusion with Respect to Claim 15

Accordingly, because neither Miyamoto nor Dortu disclose “delay elements providing different delay times for the second delay element for different frequency ranges” or “at least one second delay element is for low frequency ranges of the clock signal, and at least one further second delay element is for high frequency ranges,” the combination of Miyamoto and Dortu does not teach each and every limitation of claim 15. Therefore, it is submitted that claim 15 is in condition for allowance.

B. Claim 22

Claim 22 has been amended to include the limitation of delay elements “providing different delay times for the second delay element for different frequency ranges” similar to claim 15. Claim 22 also includes the limitation of “at least one second delay element is for low frequency ranges of the clock signal, and at least one further second delay element is for high frequency ranges.” Therefore, the arguments for patentability presented above in connection with claim 15 are applicable to claim 22. Thus, for at least the reasons discussed above with respect to claim 15, claim 22 is in condition for allowance as well.

III. Dependent Claims 16, 19-21, 25, 26 and 34-38

Claims 16, 19-21, 25, 26, 28 and 34-38 were rejected as allegedly being unpatentable over Miyamoto in view of Dortu or over Miyamoto in view of Dortu in further view of Li.

However, claims 16, 19-21, 25, 26, 28 and 34-38 depend from and incorporate all the limitations of one of independent claims 15 or 22. As set forth above, it is respectfully submitted that independent claims 15 and 22 are allowable. Accordingly, it is also respectfully submitted that dependent claims 16, 19-21, 25, 26, 28 and 34-38 are also allowable for at least the same reasons that independent claims 15 and 22 are allowable.

IV. Conclusion

Applicant respectfully requests entry of the amendment and favorable consideration of the application. A prompt and favorable action on the merits is requested.

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Respectfully Submitted,



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